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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Docket No: A7675

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Albert E. CASAVANT, et al.

MAY 11 2004

Appln. No.: 09/693,976

Group Art Unit: 2121

Technology Center 2100

Confirmation No.: 8676

Examiner: Aaron C. PEREZ DAPLE

Filed: October 23, 2000

For: PROPERTY-SPECIFIC TESTBENCH GENERATION FRAMEWORK FOR DESIGN
VALIDATION BY GUIDED SIMULATION

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.97 and 1.98

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant hereby notifies the U.S. Patent and Trademark Office of the documents which are listed on the attached PTO/SB/08 A & B (modified) form and/or listed herein and which the Examiner may deem material to patentability of the claims of the above-identified application.

One copy of each of the listed documents is submitted herewith except for:

- 1) K.L. Mc Millan, Symbolic Model Checking, Kluwer Academic Publishers, 1993.
- 2) R.P. Kurshan, Computer Aided Verification of Coordinating Processes: The Automated Approach, Princeton University., Press 1995.

Applicant thanks the Examiner for obtaining copies of these references from the U.S. Patent and Trademark Office library. Therefore, a copy of these two references is not submitted.

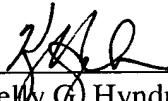
INFORMATION DISCLOSURE STATEMENT
U.S. Appln. No.: 09/693,976

The present Information Disclosure Statement is being filed (without a Statement Under 37 C.F.R. § 1.97(e)) after the later of three months from the application's filing date and the mailing date of the first Office Action on the merits, but before a Final Office Action, Notice of Allowance, or an action that otherwise closes prosecution in the application (whichever is earlier), and therefore a check for the fee of \$180.00 under 37 C.F.R. § 1.17(p) is attached.

The submission of the listed documents is not intended as an admission that any such document constitutes prior art against the claims of the present application. Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed document as a competent reference against the claims of the present application.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this paper is attached.

Respectfully submitted,



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Date: May 6, 2004

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Application Number	09/693,976
Confirmation Number	8676
Filing Date	October 23, 2000
First Named Inventor	Albert E. CASAVANT
Art Unit	2121
Examiner Name	Aaron C. PEREZ DAPLE
Attorney Docket Number	A7675

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STATEMENT BY APPLICANT**

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city, and/or country where published.	Translation ⁶
		F. Balarin, et al., "An iterative approach to language containment," In Proceedings of the International Conference on Computer-Aided Verification, volume 697 of Lecture Notes in Computer Science, pages 29--40, 1993.	
		R. K. Brayton et al., "VIS: A system for verification and synthesis", In R. Alur and T. Henzinger, editors, Proceedings of the International Conference on Computer-Aided Verification, volume 1102, pages 428--432. Springer-Verlag, June 1996.	
		R. E. Bryant, "Graph-based algorithms for Boolean function manipulation", IEEE Transactions on Computers, C-35(8):677--691, Aug. 1986.	
		J. R. Burch, E. M. Clarke, D. E. Long, K. L. McMillan, and D. L. Dill, "Symbolic model checking for sequential circuit verification", IEEE Transactions on Computer-Aided Design, 13(4):401--424, Apr. 1994.	
		A. K. Chandra, et al., "Avpgen -- a test case generator for architecture verification", IEEE Transactions on VLSI Systems, 6(6), June 1995.	
		E. M. Clarke, et al., "Automatic verification of finite-state concurrent systems using temporal logic specifications", ACM Transactions on Programming Languages and Systems, 8(2):244--263, Apr. 1986.	
		E. M. Clarke, et al., "Counterexample-guided abstraction refinement", In Proceedings of the International Conference on Computer-Aided Verification, volume 1855 of Lecture Notes in Computer Science, pages 154--169, 2000.	
		F. Fallah, et al., "Functional vector generation for HDL models using linear programming and 3-Satisfiability", In Proceedings of the Design Automation Conference, pages 528--533, San Francisco, CA, June 1998.	
		M. Ganai, et al., "Augmenting simulation with symbolic algorithms", In Proceedings of the Design Automation Conference, June 1999.	
		D. Geist, et al., "Coverage-directed test generation using symbolic techniques", In Proceedings of the International Conference on Formal Methods in CAD, pages 143--158, Nov. 1996.	
		R. C. Ho, et al., "Architecture validation for processors", In Proceedings of the 22nd Annual International Symposium on Computer Architecture, June 1995.	
		Y. Hoskote, et al., "Coverage estimation for symbolic model checking", In Proceedings of the Design Automation Conference, pages 300--305, June 1999.	
		Y. Hoskote, et al., "Automatic extraction of the control flow machine and application to evaluating coverage of verification vectors", In Proceedings of the International Conference on Computer Design, pages 532--537, Oct. 1995.	
		C.-Y. Huang, et al., "Assertion checking by combined word-level ATPG and modular arithmetic constraint-solving techniques", In Proceedings of the Design Automation Conference, pages 118--123, 2000.	
		C. N. Ip, et al., "Using symbolic analysis to optimize explicit reachability analysis", In Proceedings of Workshop on High Level Design Validation and Test, 1999.	
		S. Katz, et al., "Have I Written Enough Properties? -- a method of comparison between specification and implementation", In Proceedings of Correct Hardware Design and Verification Methods (CHARME), volume 1703 of Lecture Notes in Computer Science, pages 280--297, Sep. 1999.	
		A. Kuehlmann, et al., "Probabilistic state space search", In Proceedings of the International Conference on Computer-Aided Design, 1999.	

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Application Number	09/693,976
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First Named Inventor	Albert E. CASAVANT
Art Unit	2123
Examiner Name	Aaron C. PEREZ DAPLE
Attorney Docket Number	A7675

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		W. Lee, et al., "Tearing based abstraction for CTL model checking", In Proceedings of the International Conference on Computer-Aided Design, pages 76--81, San Jose, CA, Nov. 1996.	
		J. Lind-Nielsen, et al., "Stepwise CTL model checking of state/event systems", In Proceedings of the International Conference on Computer-Aided Verification, volume 1633 of Lecture Notes in Computer Science, pages 316--327. Springer-Verlag, 1999.	
		D. E. Long, Model Checking, Abstraction and Modular Verification, PhD thesis, School of Computer Science, Carnegie Mellon University, Pittsburgh, PA, July 1993.	
		A. Pardo, et al., "Automatic abstraction techniques for propositional μ -calculus model checking", In Proceedings of the International Conference on Computer Aided Verification, volume 1254 of Lecture Notes in Computer Science, pages 12--23, June 1997.	
		R. Sumners, et al., "Improving witness search using orders on states", In Proceedings of the International Conference on Computer Design, pages 452--457, 1999.	
		Synopsys, Inc. VERA System Verifier, http://www.synopsys.com/products/vera/vera.html	
		TransEDA, Inc. Verification Navigator, http://www.transeda.com	
		Verisity Design, Inc. Specman Elite, http://www.verisity.com/html/specmanelite.html	
		K. Wakabayashi, "C-based Synthesis Experiences with a Behavior Synthesizer "Cyber" ", In Proceedings of the Design Automation and Test in Europe (DATE) Conference, pages 390--393, 1999.	
		C. Han Yang, et al., David L. Dill, "Validation with guided search of the state space", In Proceedings of the Design Automation Conference, June 1998.	
		J. Yuan, et al., "On combining formal and informal verification", In Proceedings of the International Conference on Computer-Aided Verification, volume 1254 of Lecture Notes in Computer Science, pages 376--387, June 1997.	

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